UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

Vervain, LLC Plaintiff, v. Western Digital Corporation; Western Digital Technologies, Inc.; and HGST, Inc. Defendants.	Civil Action No. 6:21-cv-488 JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Vervain, LLC ("Vervain") asserts the following claims for patent infringement against Defendants Western Digital Corporation; Western Digital Technologies, Inc.; and HGST, Inc. (collectively "Western Digital" or "Defendants"), and alleges as follows.

NATURE OF THE ACTION

1. This is a civil action for infringement under the patent laws of the United States of America, 35 U.S.C. § 1 *et seq.*

2. Vervain is the owner of all rights, title, and interest in U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; and 10,950,300 (collectively, the "Asserted Patents").

3. Defendants have infringed and continue to infringe one or more claims of Vervain's Asserted Patents by making, using, offering to sell, and selling within the United States, and importing into the United States, including in this District, certain flash-based solid state drives ("SSDs"). Vervain seeks injunctive relief and monetary damages.

THE PARTIES

4. Plaintiff Vervain is a Texas limited liability company with its principal place of business located at 7424 Mason Dells Drive, Dallas, Texas 75230.

5. Defendant Western Digital Corporation ("WDC") is a Delaware corporation with a principal place of business at 5601 Great Oaks Parkway, San Jose, CA 95119. Either directly or through its subsidiaries, WDC also has a place of business at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731. WDC can be served through its registered agent, the Corporation Service Company at 251 Little Falls Drive, Wilmington, Delaware 19808.

6. Defendant Western Digital Technologies, Inc. ("WDT") is a subsidiary of WDC. WDT is a Delaware corporation with a principal place of business at 5601 Great Oaks Parkway, San Jose, CA 95119. WDT also has a place of business at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731. WDT is registered with the Texas Secretary of State to do business in Texas. WDT can be served through its registered agent, The Corporation Service Company d/b/a CSC-Lawyers Incorporating Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

7. Defendant HGST, Inc. ("HGST") is a subsidiary of WDC. HGST is a Delaware corporation with a principal place of business at 5601 Great Oaks Parkway, San Jose, CA 95119. HGST also has a place of business at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731. HGST is registered with the Texas Secretary of State to do business in Texas. HGST can be served through its registered agent, The Corporation Service Company d/b/a CSC-Lawyers Incorporating Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

8. Western Digital is a developer, manufacturer, and provider of data storage devices and solutions, including flash-based solid state drives ("SSDs").[1] Western Digital offers a broad line of storage solutions, including client devices; data center devices and solutions; and client solutions.[2]

9. The client devices include SSDs for computing devices, such as desktop and notebook PCs, smart video systems, gaming consoles and set top boxes; and flash-based embedded storage products for mobile phones, tablets, notebook PCs and other portable and wearable devices, automotive, Internet of Things ("IoT"), industrial and connected home applications.[3]

10. The data center devices and solutions include high-performance flash-based SSDs and software solutions that are optimized for performance applications providing a range of capacity and performance levels primarily for use in enterprise servers, supporting high volume on-line transactions, data analysis and other enterprise applications.[4]

11. The client solutions include SSDs embedded into external storage products and removable flash-based products, which include cards, universal serial bus ("USB") flash drives and wireless devices. Western Digital offers client portable SSDs with a range of capacities and performance characteristics to address a broad spectrum of the client storage market. The removable cards are designed primarily for use in consumer devices, such as mobile phones, tablets, imaging systems, still cameras, action video camera and smart video systems. The USB

[1] Western Digital's 2020 Annual Report, available at https://investor.wdc.com/financial-information/annual-reports (last visited April 21, 2021), at 5.
[2] *Id*. at 7.
[3] *Id*.
[4] *Id*.

flash drives are used in the computing and consumer markets and are designed for high-performance and reliability. The wireless drive products allow in-field back up of created content, as well as streaming of high-definition movies, photos, music and documents to tablets, smartphones, and PCs.[5]

12. Western Digital's products are offered under the Western Digital, G-Technology, HGST, SanDisk, Upthere, and WD brands. Western Digital sells its products to customers, including customers in this District, in the computer, networking and storage, consumer electronics, and mobile telecommunications markets.

13. Western Digital maintains offices in Austin, Texas. Within the United States, Western Digital also has offices in Irvine, Milpitas Newark, Redwood City and San Jose, California.[6] Outside the United States, Western Digital has offices in China, India, Japan, South Korea, Singapore, Taiwan, Belgium, Israel, and the United Kingdom.[7] Western Digital operates manufacturing facilities in the United States, Malaysia, and China and manufactures SSDs in at least Malaysia and China.[8]

14. Western Digital operates and owns the westerndigital.com website, and markets, offers, distributes, and provides technical support for its SSDs throughout the United States including in this District.

15. Each of the Defendants develops, designs, manufactures, distributes, markets, offers to sell, or sells infringing products or services within the United States, including in this District, and otherwise purposefully directs infringing activities to this District in connection

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[5] *Id*.
[6] Ex. E, https://www.westerndigital.com/office-locations (printed April 12, 2021).
[7] *Id*.
[8] Ex. F, https://www.anandtech.com/show/13097/western-digital-to-shut-down-hdd-manufacturing-facility-increase-production-of-ssds (printed April 21, 2021).

with its Austin, Texas offices; its westerndigital.com website; and its other places of business in Texas and the rest of the United States.

16. Defendants have been and are acting in concert, and are otherwise liable jointly, severally, or otherwise for relief related to or arising out of the same transaction, occurrence, or series of transactions or occurrences related to the making, using, selling, offering for sale, or otherwise distributing the SSDs in this District.

17. In addition, this action involves questions of law and fact that are common to all Defendants. For example, Defendants are making, using, offering for sale, selling, or otherwise distributing at least some of the SSDs in this District.

JURISDICTION AND VENUE

18. This is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*. This Court has subject matter jurisdiction over the matters asserted in this Complaint under 28 U.S.C. §§ 1331 and 1338(a) and 35 U.S.C. §§ 271 *et seq*.

19. This Court has personal jurisdiction over Defendants in accordance with due process and/or the Texas Long Arm Statute because, in part, Defendants "recruit[] Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state." Tex. Civ. Prac. & Rem. Code § 17.042(3).

20. This Court has personal jurisdiction over Defendants, in part because Defendants do continuous and systematic business in this District, including by providing infringing products and services to residents of this District that Defendants knew would be used within this District, and by soliciting business from residents of this District.

21. For example, Defendants are subject to personal jurisdiction in this Court because, *inter alia*, they have regular and established places of business in this District, including an office located at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731.

22. The Travis Central Appraisal District (CAD) website[9] indicates that for tax year 2016, SanDisk Corporation Austin (d/b/a Western Digital Technologies, Inc.) and Hitachi Global Storage Technologies, Inc. (d/b/a HGST) owned property at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731. In addition, WDT owned property at 3600 W. Parmer Lane, Suite 2-160, Austin, Texas 78728, as well as various locations.[10]

23. In tax year 2017, WDT and HGST owned property at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731. In addition, WDT owned property at 3600 W. Parmer Lane, Suite 2-160, Austin, Texas 78728, as well as various locations.[11]

24. In tax year 2018, WDT owned property at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731, as well as various locations.[12]

25. In tax years 2019, 2020, and 2021, WDT owned and continues to own property at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731; 19000 Limestone Commercial Drive, Suite 500, Pflugerville, Texas 78660; as well as various locations.[13]

26. As shown in the following picture taken on April 15, 2021, Western Digital does business at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731 under the names Western Digital, HGST, and SanDisk.

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[9] https://www.traviscad.org/property-search/ (last visited April 21, 2021); http://propaccess.traviscad.org/clientdb/?cid=1 (last visited April 21, 2021).
[10] Ex. G, http://propaccess.traviscad.org/clientdb/SearchResults.aspx (printed April 22, 2021) (property search results for Western Digital and HGST for 2016).
[11] Ex. H, http://propaccess.traviscad.org/clientdb/SearchResults.aspx (printed April 22, 2021) (property search results for Western Digital and HGST for 2017).
[12] Ex. I, http://propaccess.traviscad.org/clientdb/SearchResults.aspx (printed April 22, 2021) (property search results for Western Digital for 2018).
[13] Ex. J, http://propaccess.traviscad.org/clientdb/SearchResults.aspx (printed April 22, 2021) (property search results for Western Digital for 2019-2021).

27. On information and belief, Western Digital has also used or continues to use property at 9442 N. Capital of Texas Highway, Austin, Texas 78759. On information and belief, a WD technical sales support team that supports a large local customer with hard drives and SSDs is located or was located at 9442 N. Capital of Texas Highway, Austin, Texas 78759.

28. Western Digital's Austin offices are regular and established places of business at least because these locations include many members of Western Digital's important teams, including research staff members and senior technologists in the CPU project group, ASIC engineers, mechanical design engineers, field application engineers, sales account executives, and customer technical support.

29. For example, on information and belief, Scott Glenn, Director of Global Channel and OEMs, works in the Austin, Texas area.[14] On information and belief, Deepak Veerapandian, Senior Engineer, Firmware Verification, works in the Austin, Texas area.[15] On information and belief, Joe Rahmeh, Senior Technologist, works in the Austin, Texas area.[16] On information and belief, Srini Vemuri, Director of RISC-V CPU Design, works in the Austin, Texas area.[17] On information and belief, Robert Golla, Senior Fellow, works in the Austin, Texas area.[18] On information and belief, Frances Fluitt, Worldwide Account Executive, works in the Austin, Texas area.[19] On information and belief, Kevin Li, Director, Customer Technical Support, works in the Austin, Texas area.[20]

30. Western Digital regularly posts job openings for its Texas office on the Western Digital website.[21] For example, Western Digital's website includes a job posting for a research staff member in the CPU development group.[22] Additional job postings can be found on LinkedIn and other websites.[23]

[14] Ex. K, https://www.linkedin.com/in/sglenn1/ (printed April 22, 2021).
[15] Ex. K, https://www.linkedin.com/in/deepak-vp/ (printed April 22, 2021).
[16] Ex. K, https://www.linkedin.com/in/joe-rahmeh-296a758/ (printed April 22, 2021).
[17] Ex. K, https://www.linkedin.com/in/srinivemuri/ (printed April 22, 2021).
[18] Ex. K, https://www.linkedin.com/in/robert-golla-0261019/ (printed April 22, 2021).
[19] Ex. K, https://www.linkedin.com/in/francesfluitt/ (printed April 22, 2021).
[20] Ex. K, https://www.linkedin.com/in/kevinli/ (printed April 22, 2021).
[21] Ex. L, https://careers.westerndigital.com/ (printed April 22, 2021).
[22] Ex. L, https://careers.westerndigital.com/jobs/senior-technologist-r-d-engineering-cpus-12174 (printed April 6, 2021).
[23] Ex. M, https://www.linkedin.com/jobs/view/senior-technologist-r-d-engineering-cpu-s-at-western-digital-2464829329 (printed April 6, 2021); https://lensa.com/director-cpu-jobs/austin/jd/d4cd86d7ba2bbe0e1eee16ee08a74815 (printed April 12, 2021).

31. Based on publicly-available information, HGST is the employer of a recipient of a H-1B visa, with a start date of October 1, 2020, who works and resides in the Austin, Texas area.[24]

32. Western Digital, directly and through agents, regularly conducts, solicits, and transacts business in this District and elsewhere in Texas, including through its Western Digital.com website. For example, Defendants employ sales and marketing employees that regularly offer to sell, sell, or otherwise distribute SSDs in this District and elsewhere in Texas.

33. In particular, Western Digital has committed and continues to commit acts of infringement in violation of 35 U.S.C. § 271, and has made, used, marketed, distributed, offered for sale, and sold infringing products in Texas, including in this District, and engaged in infringing conduct within and directed at or from this District. The infringing SSDs have been and continue to be distributed to and used in this District. Western Digital's acts cause injury to Vervain, including injury suffered within this District.

34. Venue is proper in this District under 28 U.S.C. §§ 1391 and 1400(b) because a substantial part of the events or omissions giving rise to the claims occurred in this District, and because Defendants have committed acts of infringement in this District and have a regular and established place of business in this District.

35. In particular, Western Digital has a regular and established place of business located at 7501 N. Capital of Texas Highway, Suite A-100, Austin, Texas 78731. Furthermore, WDT and HGST are registered to do business in Texas.

[24] Ex. N, https://h1bdata.info/index.php?em=HGST+INC&job=&city=AUSTIN&year=ALL+YEARS (printed April 22, 2021)

36. WDT and HGST are wholly owned subsidiaries of WDC. WDC does not separately report revenue from WDT or HGST in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various products and subsidiaries.

37. On information and belief, WDC not only "owns" but also "operates" WDT and HGST, including the cooperative development, improvement, and support of Western Digital's products and services.

VERVAIN'S ASSERTED PATENTS

38. U.S. Patent No. 8,891,298 (the "'298 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 18, 2014. A true and correct copy of the '298 patent is attached as Exhibit A to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '298 patent, with the full and exclusive right to bring suit to enforce the '298 patent, including the right to recover for past infringement. The '298 patent is valid and enforceable under United States patent laws.

39. U.S. Patent No. 9,196,385 (the "'385 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 24, 2015. A true and correct copy of the '385 patent is attached as Exhibit B to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '385 patent, with the full and exclusive right to bring suit to enforce the '385 patent, including the right to recover for past infringement. The '385 patent is valid and enforceable under United States patent laws.

40. U.S. Patent No. 9,997,240 (the "'240 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on June 12, 2018. A true and correct copy of the '240 patent is attached as Exhibit C to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '240 patent, with the full and exclusive right to bring suit to enforce the

'240 patent, including the right to recover for past infringement. The '240 patent is valid and enforceable under United States patent laws.

41. U.S. Patent No. 10,950,300 (the "'300 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on March 16, 2021. A true and correct copy of the '300 patent is attached as Exhibit D to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '300 patent, with the full and exclusive right to bring suit to enforce the '300 patent, including the right to recover for past infringement. The '300 patent is valid and enforceable under United States patent laws.

42. G.R. Mohan Rao is the sole inventor of the Asserted Patents.

43. Dr. Rao is the inventor of approximately 111 U.S. patents and the author of at least 15 technical publications spanning several decades.

44. Dr. Rao has been an innovator in the semiconductor industry since the 1960s. After receiving his Ph.D. in physics with a specialization in electronics in September 1968 from Andhra University in Waltair, India, near the village where he grew up, Dr. Rao traveled to the United States to attend a graduate program in physics at the University of Cincinnati, fulfilling his lifelong dream to study in the United States.

45. Shortly after beginning his studies at the University of Cincinnati, Dr. Rao found a bulletin indicating that Prof. William Carr of Southern Methodist University (SMU) was looking for a graduate assistant for his work on MOS transistors. Dr. Rao called Prof. Carr about the opportunity, and by December 1968, after completing the fall semester at the University of Cincinnati, Dr. Rao had received the assistantship with Prof. Carr, moved to Dallas, Texas, and enrolled in a Ph.D. program at SMU in electrical engineering.

46. At the laboratory at SMU, Dr. Rao was able to build MOS devices from scratch. In the 1969-1970 timespan, while attending SMU, Dr. Rao also worked in the SMU laboratory with Jack Kilby of Texas Instruments, a pioneering electrical engineer who would later receive a Nobel Prize for his work. In early 1972, Mr. Kilby set up an interview for Dr. Rao at Texas Instruments' Houston facility, then the home of Texas Instruments' MOS-related work.

47. Dr. Rao began working for Texas Instruments in June 1972. He would go on to work for the company for 22 years, until 1994. Dr. Rao rose through the ranks at Texas Instruments, starting in an Engineer position and ascending to the position of Senior Fellow—one of 12 out of approximately 20,000 engineers at the company at the time. He then moved into a management position, starting as a Vice President in 1983 and becoming a Senior Vice President in 1985.

48. Dr. Rao received his first patent while working in a process and product engineering capacity to solve a production problem with Texas Instruments' 4-kilobit RAM product. From the late 1970s through the mid-1980s, he worked on and/or managed Texas Instruments': (1) 64Kb RAM, in a project management capacity as a Senior Member of Technical Staff; (2) 256Kb RAM, in a project management capacity as a Fellow; (3) 1Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects; and (4) 4Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects. At Texas Instruments, Dr. Rao also worked on projects involving EEPROM, SRAM, and microcontrollers. In total, Dr. Rao received approximately 35 U.S. patents during his time at Texas Instruments.

49. Some of Dr. Rao's work for Texas Instruments is featured in the Smithsonian Institution, in the Texas Instruments Collection.[25] For example, the Smithsonian Institution has a display of Texas Instruments' experimental 1-megabit CMOS DRAM with one-Western Digital feature size, produced in April 1985 under Dr. Rao's leadership.

50. After his time at Texas Instruments, Dr. Rao joined Cirrus Logic in 1994. Although Cirrus Logic was a California company, Dr. Rao coordinated a team in the Dallas area. His work focused on a major project involving integration of a graphics controller and memory. During his time at Cirrus Logic, Dr. Rao received approximately 22 U.S. patents relating to his work on integrated graphics controllers and memory. Dr. Rao left Cirrus Logic in the summer of 1996.

51. Later in 1996, Dr. Rao started a company called Silicon Aquarius. Through a relationship between Silicon Aquarius and Matsushita, Dr. Rao led a design team in working on a 256Mb DRAM chip.

52. After Silicon Aquarius ceased operations, Dr. Rao did consulting work for a number of different companies and devoted much of his free time to thinking about various challenges and problems with which the semiconductor industry had struggled for years. For example, Dr. Rao worked to improve non-volatile memories that are used for long term storage of data after the power is turned off, and how to reduce the power consumption of those devices.

53. In non-volatile memories, there are two types of storage cells: single-level cells (SLCs) that store one bit of information, and multi-level cells (MLCs) that store multiple bits of information. SLCs are faster, more reliable, and have a longer life. MLCs are less expensive

[25] http://smithsonianchips.si.edu/texas/t_360.htm (last visited Apr. 12, 2021); http://smithsonianchips.si.edu/texas/wafer.htm (last visited Apr. 12, 2021).

and can store more data in less space with less power consumption. While working to improve these non-volatile memories, Dr. Rao developed inventions that combine the long life and high-performance of SLCs with the more cost-effective MLCs. The result is the best of both types of cells – longer life and better performance at less cost. By using the MLCs as the default storage, the cheaper, more reliable MLCs are used for the bulk of the data storage. Meanwhile, the SLCs are used for the data that needs it the most.

54. The claims of the Asserted Patents are directed to patent-eligible, non-abstract ideas. They address, among other things, specific improvements for controlling non-volatile memory modules. The claims are particularly useful for flash memory products or other memory devices that use a combination of SLCs and multi-level cells MLCs. If, for example, a range of addresses in a MLC memory module fails a data integrity test, the range of addresses may be mapped to a new range of addresses in a SLC memory module. Also, if a block in the MLC module is used frequently, the block may be transferred to the SLC module. By doing so, the reliability and life of the flash memory is increased.

55. Vervain's Asserted Patents claim, among other things, a specific implementation of a solution to a problem in the design and fabrication of flash memories. For example, the patents identify numerous specific advantages that Vervain's claimed techniques provide compared to traditional forms of flash memories. *See, e.g.*, Ex. A, '298 patent at 1:25-32; Ex. B, '385 patent at 1:28-35; Ex. C, '240 patent at 1:40-47; Ex. D, '300 patent at 1:44-51. Further, the claimed technologies cannot be performed as mental steps by a human, nor do they represent the application of a generic computer to any well-known method of organizing human behavior.

56. The Asserted Patents claim inventive concepts that are significantly more than any patent-ineligible, abstract idea. In particular, the claimed technologies, including individual

limitations as well as ordered combinations of limitations, were not well-understood, routine, or conventional, and cover multiple advantages, and combinations of advantages, that were not well-understood, routine, or conventional. *See, e.g.*, Ex. A, '298 patent at 5:24-40, 6:24-35; Ex. B, '385 patent at 5:28-44, 6:28-39; Ex. C, '240 patent at 5:43-59, 6:46-58; Ex. D, '300 patent at 5:51-67, 6:53-65.

DEFENDANTS' INFRINGING PRODUCTS AND ACTIVITIES

57. Western Digital is a developer, manufacturer, and provider of data storage devices and solutions, including flash-based solid state drives ("SSDs"). Western Digital designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes SSDs for a wide array of uses, including client devices; data center devices and solutions, and client solutions.

58. Western Digital designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes, and provides support for SSDs, including products with the part name or number WD Blue 3D NAND SATA SSD WDS250G2B0A, SanDisk Ultra 3D SSD SDSSDH3-250G-G25, SanDisk X600 3D NAND SATA SSD, WD Black 3D NAND SSD SN750, SanDisk Extreme PRO M.2 NVMe 3D SSD, WD PC SN520 NVMe SSD, WD PC SN530 NVMe SSD, WD PC SN730 NVMe SSD, WD Blue SN550 NVMe SSD WDS250G2B0C, and WD Black NVMe SSD SN850, and other memory products that have the same or similar structures, features, or functionalities, as the aforementioned products ("Accused Products").

59. The Accused Products are integrated into devices made, used, offered for sale, sold, imported, supplied, or otherwise distributed in the United States by among others, Western Digital, Western Digital's customers, original equipment manufacturers ("OEMs"), original design manufacturers ("ODMs"), foundry suppliers, distributers, and other third parties. Western Digital's Accused Products are essential, non-trivial components of the products into which they are integrated.

60. Western Digital also conducts research, development, and testing of Accused Products in the United States.

61. Western Digital maintains a website that advertised and continues to advertise the Accused Products, including identifying the applications for which they can be used and specifications for the Accused Products.

62. Western Digital's development, sales, marketing, and manufacturing activities in the United States, including within this District, directly contributed to Western Digital's net revenue in the United States.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 8,891,298

63. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

64. Defendants have directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '298 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

65. The Accused Products meet all the limitations of at least claim 1 of the '298 patent. Specifically, claim 1 of the '298 patent recites:

> A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to:

a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

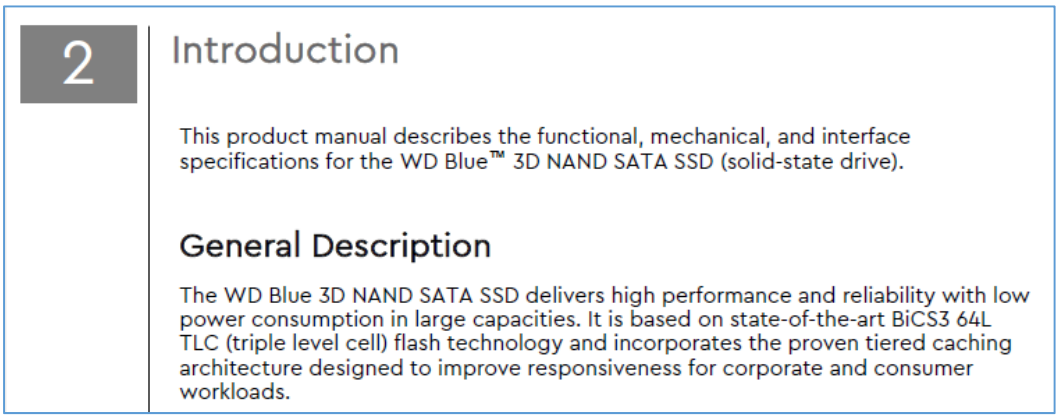
c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and

d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

66. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, Western Digital's Blue 3D NAND SATA SSD product number WDS250G2B0A ("WDS250G2B0A") is a solid state drive (SSD) for storing data.

Western Digital Store[26]*; see also White Paper at 1, 4.*[27]

67. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, WDS250G2B0A comprises TLC (triple level cell) flash technology.



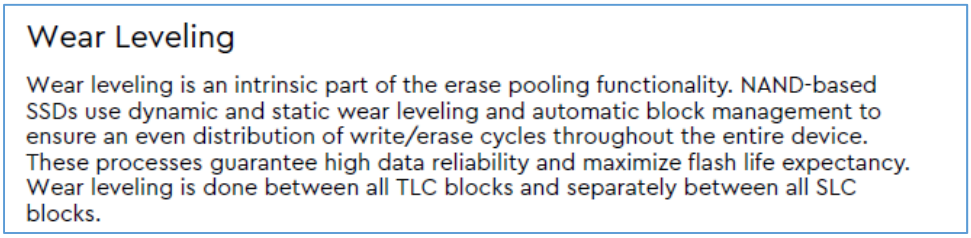
2 Introduction

This product manual describes the functional, mechanical, and interface specifications for the WD Blue™ 3D NAND SATA SSD (solid-state drive).

General Description

The WD Blue 3D NAND SATA SSD delivers high performance and reliability with low power consumption in large capacities. It is based on state-of-the-art BiCS3 64L TLC (triple level cell) flash technology and incorporates the proven tiered caching architecture designed to improve responsiveness for corporate and consumer workloads.

User Manual at 2.[28] The SSD is configured to erase TLC blocks.



Wear Leveling

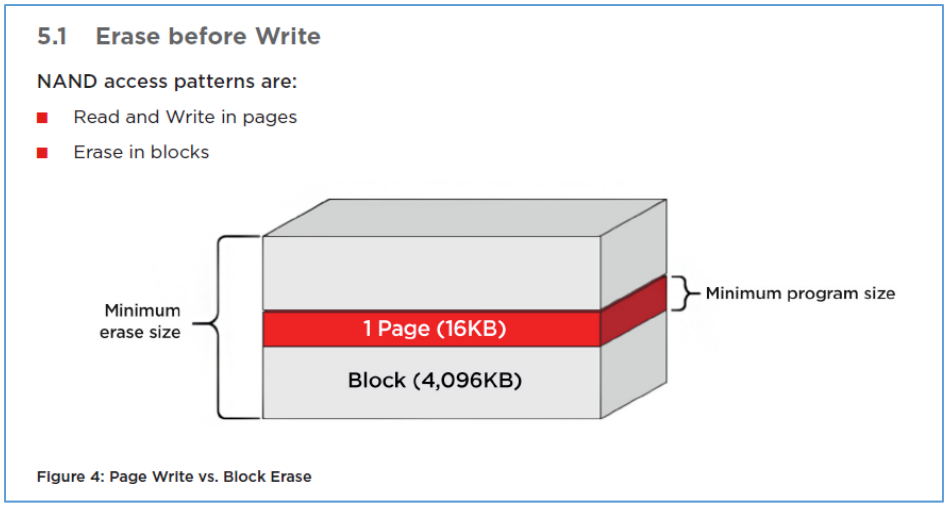
Wear leveling is an intrinsic part of the erase pooling functionality. NAND-based SSDs use dynamic and static wear leveling and automatic block management to ensure an even distribution of write/erase cycles throughout the entire device. These processes guarantee high data reliability and maximize flash life expectancy. Wear leveling is done between all TLC blocks and separately between all SLC blocks.

Id. at 4.

[26] Ex. O, Western Digital Store for WD Blue SATA SSD ("*WD Store*"), available at https://shop.westerndigital.com/products/internal-drives/wd-blue-sata-2-5-ssd#WDS250G2B0A (printed April 22, 2021).

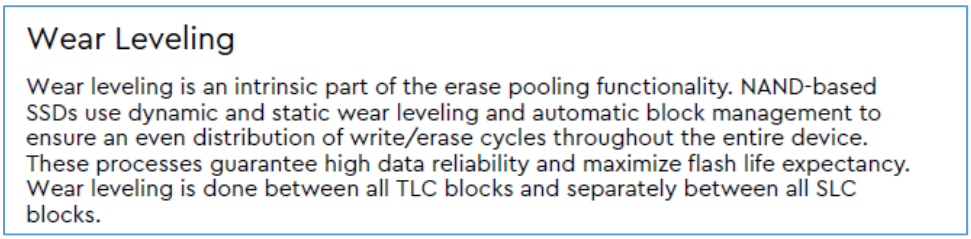
[27] Ex. P, SanDisk White Paper, Flash 101 and Flash Management: A detailed overview of flash and flash management techniques, Oct. 2016 ("White Paper"), available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf (last visited April 22, 2021).

[28] Ex. Q, WD Blue 3D NAND SATA SSD Internal SSD Storage User Manual ("*User Manual*"), available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/internal-drives/wd-blue-ssd/user-manual-wd-blue-3d-nand-sata-ssd.pdf (last visited April 22, 2021).

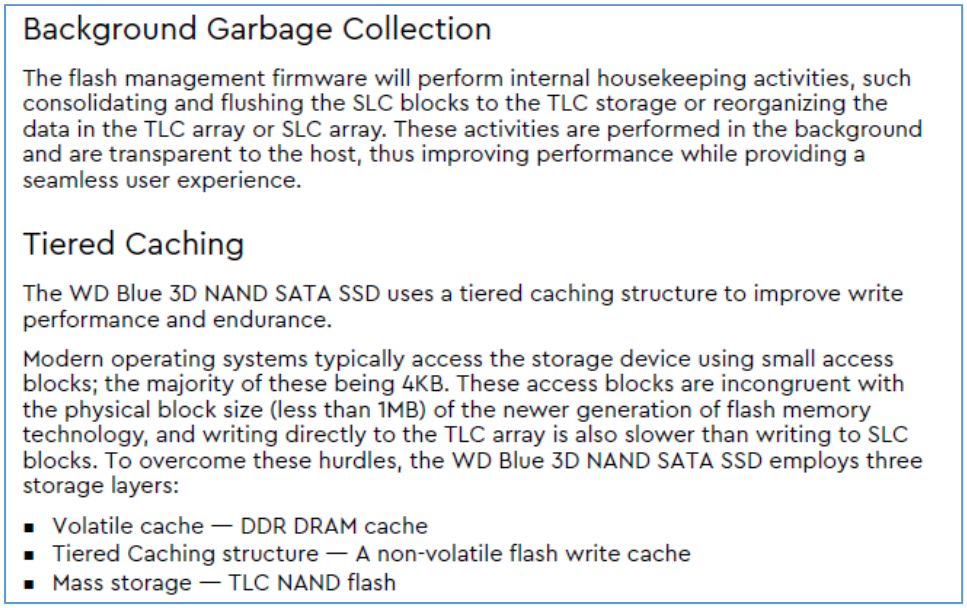


White Paper at 8.

68. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, WDS250G2B0A is configured to erase SLC blocks.



User Manual at 4.



Background Garbage Collection

The flash management firmware will perform internal housekeeping activities, such consolidating and flushing the SLC blocks to the TLC storage or reorganizing the data in the TLC array or SLC array. These activities are performed in the background and are transparent to the host, thus improving performance while providing a seamless user experience.

Tiered Caching

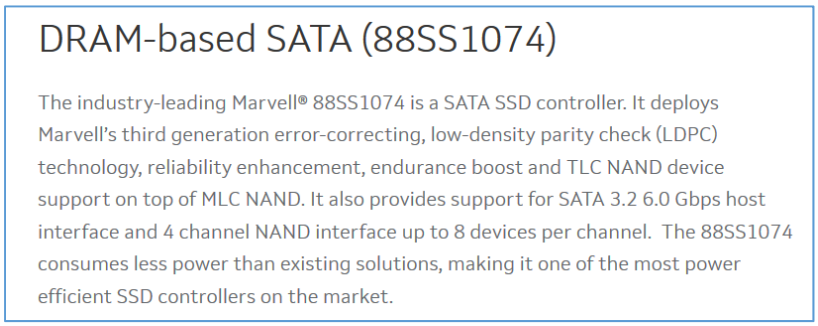
The WD Blue 3D NAND SATA SSD uses a tiered caching structure to improve write performance and endurance.

Modern operating systems typically access the storage device using small access blocks; the majority of these being 4KB. These access blocks are incongruent with the physical block size (less than 1MB) of the newer generation of flash memory technology, and writing directly to the TLC array is also slower than writing to SLC blocks. To overcome these hurdles, the WD Blue 3D NAND SATA SSD employs three storage layers:

- Volatile cache — DDR DRAM cache
- Tiered Caching structure — A non-volatile flash write cache
- Mass storage — TLC NAND flash

Id. at 5.

69. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module. For example, WDS250G2B0A contains a controller with a NAND interface.



DRAM-based SATA (88SS1074)

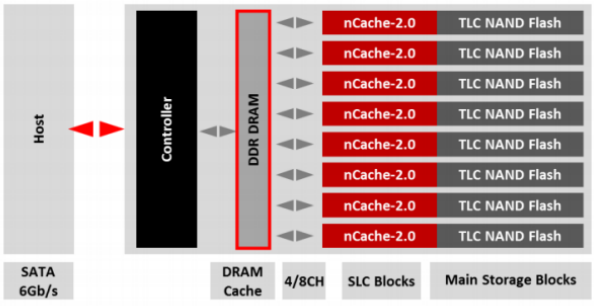
The industry-leading Marvell® 88SS1074 is a SATA SSD controller. It deploys Marvell's third generation error-correcting, low-density parity check (LDPC) technology, reliability enhancement, endurance boost and TLC NAND device support on top of MLC NAND. It also provides support for SATA 3.2 6.0 Gbps host interface and 4 channel NAND interface up to 8 devices per channel. The 88SS1074 consumes less power than existing solutions, making it one of the most power efficient SSD controllers on the market.

Controller.[29] The controller uses nCache technology.

[29] Exhibit R, Marvell, SATA SSD Controllers, DRAM-based SATA (88SS1074) ("*Controller*"), available at https://www.marvell.com/products/ssd-controllers/88ss1074.html (printed April 23, 2021).

SanDisk nCache 2.0 Technology

SanDisknCache 2.0 is a proprietary pseudo-SLC caching technology that greatly increases the *write performance* of the solid state drive. Here is an old infographic (from their Ultra II SSD) that shows how it works :



A small portion (about 4%) of the NAND memory blocks are set to run in the **SLC mode**, which allows for a much higher write speed. This SLC portion serves as a **fast write cache** for all writes to the drive, allowing for write speeds of **up to 530 MB/s**.

nCache 2.0.[30]

2.4.5 SLC Cache - nCache 3.0

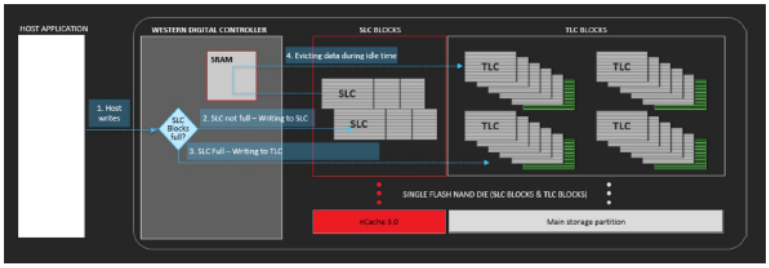
The nCache 3.0 is a pool of X1 (SLC) blocks for sequential and random host operations. These X1 blocks are used as write cache to accumulate and consolidate all writes at high speed.

The PC SN730 NVME SSD utilize the nCache 3.0 tiered caching which further improves performance and power efficiently by introducing several enhancements as:

- Direct TLC (write) Access - improves sustain-write-access power efficiency and write throughput.
- Enhanced Evacuation Policy - improves the write-burst access speed.

As mentioned above, the nCache 3.0 works in the background to flush them into the larger X3 (TLC) storage blocks and uses optimized write transaction sizes to maximize endurance. Once the SLC blocks are full the Drive will continue to program TLC blocks directly, and will re-locate the data from SLC to TLC on Idle times.

Figure 2-1. Western Digital PC SN730 NVMe SSD Tiered Caching Technology



nCache 3.0 at 11. [31]

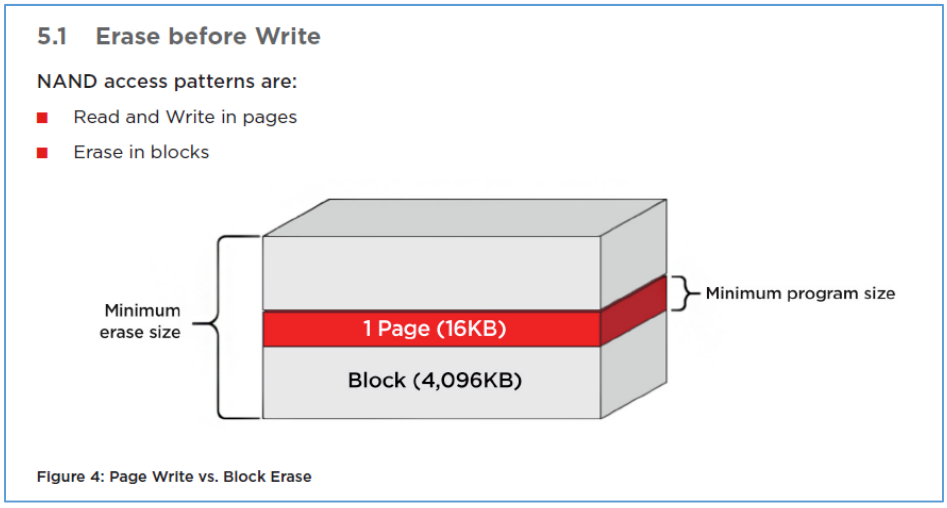
[30] Exhibit S, TechARP, The 1TB WD Blue 3D SSD (WDS100T2B0A) Review ("*nCache 2.0*"), available at https://www.techarp.com/reviews/1tb-wd-blue-3d-ssd-review/2/ (printed April 23, 2021).

[31] Exhibit T, Western Digital, Product Manual, PC SN730 NvMe SSD ("*nCache 3.0*"), available at https://downloads.sandisk.com/downloads/um/pcsn730-pm.pdf (last visited April 23, 2021).

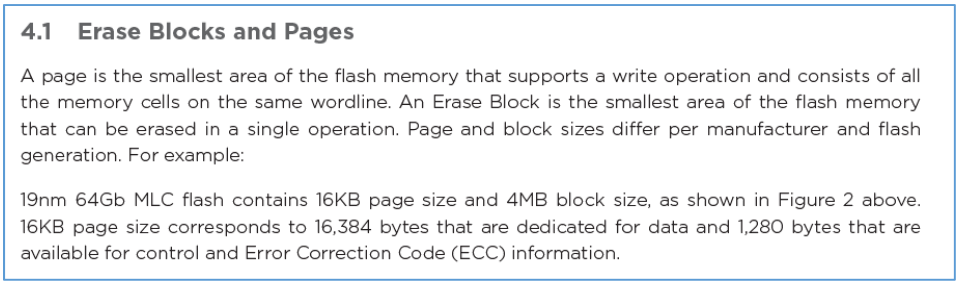
70. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, WDS250G2B0A uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory.

- The managed NAND controller has the ability to map an LBA address to different physical locations on the flash. The controller uses a mapping table to keep track of the relationship between the logical block and the physical address

White Paper at 12. The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit.



White Paper at 8.



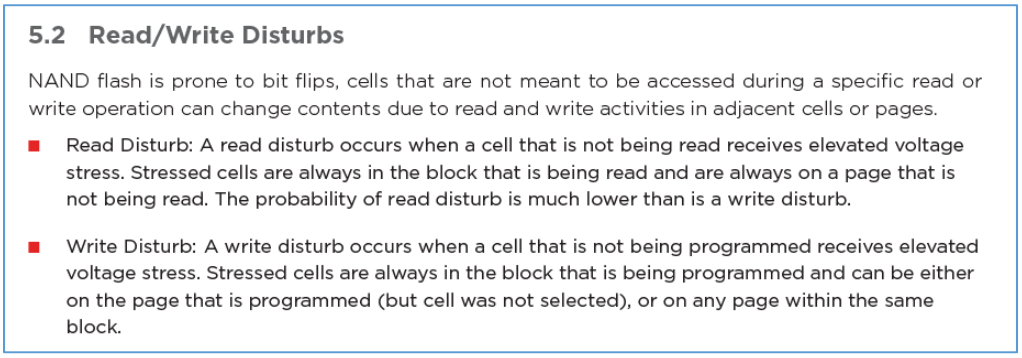
4.1 Erase Blocks and Pages

A page is the smallest area of the flash memory that supports a write operation and consists of all the memory cells on the same wordline. An Erase Block is the smallest area of the flash memory that can be erased in a single operation. Page and block sizes differ per manufacturer and flash generation. For example:

19nm 64Gb MLC flash contains 16KB page size and 4MB block size, as shown in Figure 2 above. 16KB page size corresponds to 16,384 bytes that are dedicated for data and 1,280 bytes that are available for control and Error Correction Code (ECC) information.

Id. at 6.

71. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, the flash memory in WDS250G2B0A is prone to read and write disturb errors.



5.2 Read/Write Disturbs

NAND flash is prone to bit flips, cells that are not meant to be accessed during a specific read or write operation can change contents due to read and write activities in adjacent cells or pages.

- Read Disturb: A read disturb occurs when a cell that is not being read receives elevated voltage stress. Stressed cells are always in the block that is being read and are always on a page that is not being read. The probability of read disturb is much lower than is a write disturb.
- Write Disturb: A write disturb occurs when a cell that is not being programmed receives elevated voltage stress. Stressed cells are always in the block that is being programmed and can be either on the page that is programmed (but cell was not selected), or on any page within the same block.

White Paper at 9. The controller implements flash management techniques to address data integrity issues by remapping data.

Five significant factors influencing reliability, performance, and write endurance of the managed NAND devices are:

- Use of Single Level Cell (SLC) vs. Multi-Level Cell (MLC) NAND flash technology
- Wear-leveling algorithms
- Ensuring data integrity through Bad Block management techniques
- Use of error detection and correction techniques
- Write amplification

Implementation of sophisticated flash management techniques that are properly implemented will deliver products with high reliability, long service life, high performance, and excellent data integrity characteristics.

Id. at 4.

Functional Description

The WD Blue 3D NAND SATA SSD supports the following features:

- Support for multi-stream – improves user experience in multitasking systems
- Support for TRIM command – sustains drive's high performance over time
- Minimal write amplification – increases endurance and performance
- Tiered caching, including use of allocated SLC blocks
- Support for ATA register and command set (ATA-8/ACS-4 standard)
- SMART feature support
- Error recovery using Error Correction Code (ECC)
- Self-management of NAND memory defects
- Advanced power management for low-power operation, including DEVSLP capability
- Error-management system - provides a last line of data protection
- Dynamic and static wear leveling to extend the life of the WD Blue 3D NAND SATA SSD

Advanced Flash Management

Defect and Error Management

The WD Blue 3D NAND SATA SSD contains an enhanced defect and error management system that is similar to systems found in hard disk drives (HDDs). If necessary, the device will rewrite data from a defective block to a good block. This action is completely transparent to the host and does not consume any user data space.

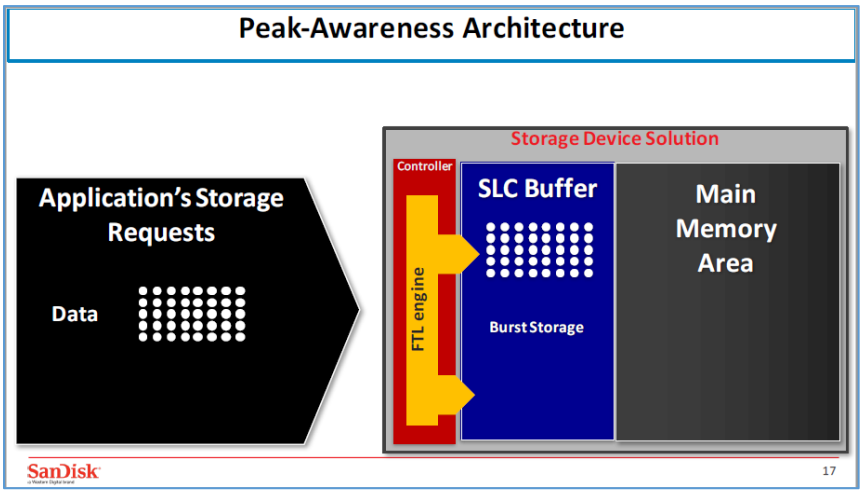
The WD Blue 3D NAND SATA SSD soft error rate specification is superior to the HDD specification. In the rare case when a read error occurs, the drive uses Error Detection Code (EDC) and Error Correction Code (ECC) algorithms to recover the data. These defect and error management systems give it unparalleled reliability.

The WD Blue 3D NAND SATA SSD also includes a robust error handling mechanism which can recover errors that other traditional error correction mechanisms cannot. This mechanism can leverage a hardware XOR core to calculate the extra parity on-the-fly with minimal impact in performance.

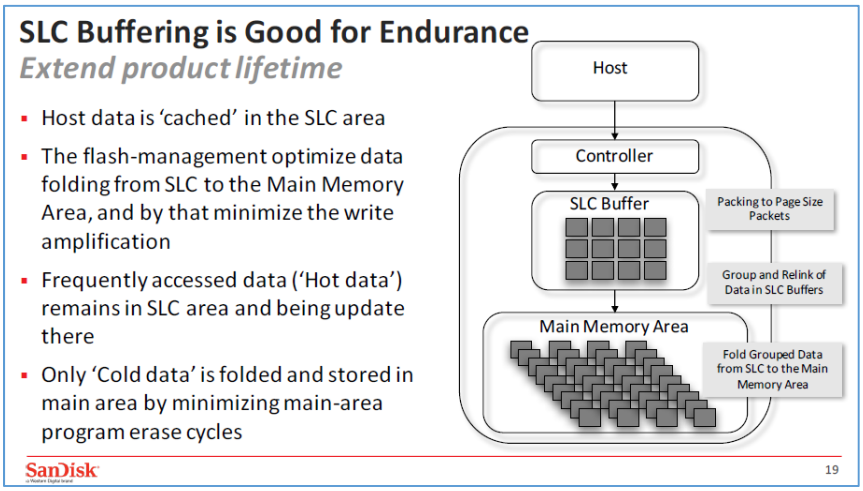
User Manual at 4.

72. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the

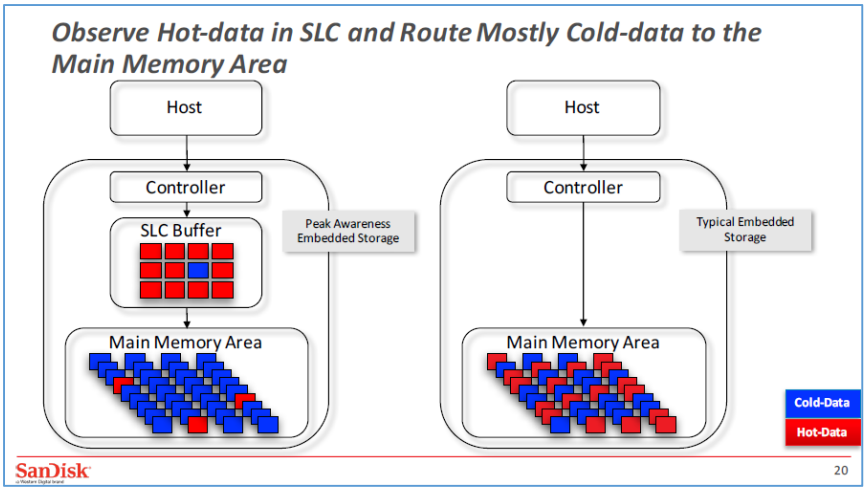
controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, the controller in WDS250G2B0A determines "hot" data and "cold" data. Hot data is stored in SLC memory and cold data is stored in MLC memory.



SanDisk Presentation at 17. [32]



[32] Ex. U, A. Lemberg, The Better Alignment of Managed Flash to System Behavior ("*SanDisk Presentation*"), available at https://events.static.linuxfound.org/sites/events/files/slides/Storage_Alignment_To_System_Behaviour_0_0.pdf (last visited April 22, 2021).

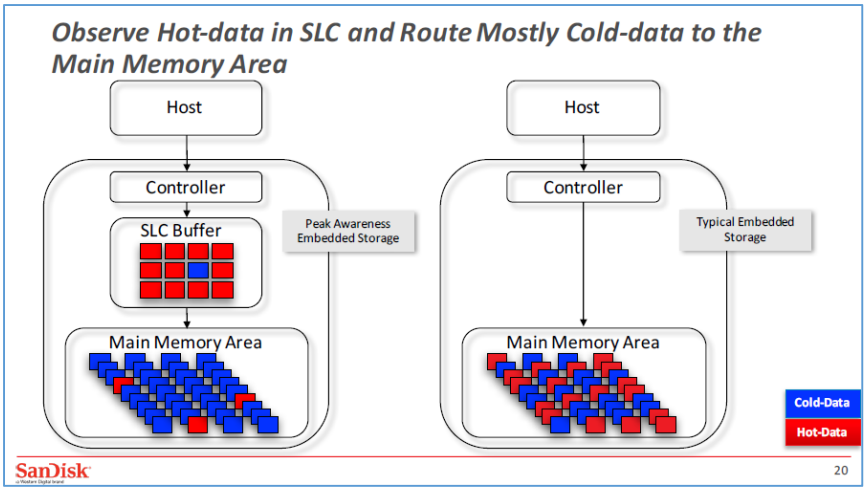


Id. at 19-20. The controller maintains a hot count of each of the physical blocks.

> ■ Hot count and other parameters of each of the physical blocks are monitored. Once those indicators cross a pre-defined threshold, the wear leveling algorithm will rotate the data to blocks that did not reach this threshold.

White Paper at 12.

73. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. For example, the controller in WDS250G2B0A determines "hot" data and "cold" data and stores the "hot" data in the SLC memory.



SanDisk Presentation at 20.

74. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

75. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

76. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '298 patent by Defendants.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 9,196,385

77. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

78. Defendants have directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '385 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on

currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

79. The Accused Products meet all the limitations of at least claim 1 of the '385 patent. Specifically, claim 1 of the '385 patent recites:

> A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a flash translation layer (FTL); wherein the FTL is adapted to:
>
> a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
>
> b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
>
> c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and
>
> d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

80. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, WDS250G2B0A is a SSD for storing data. *Western Digital Store; see also White Paper at 1, 4.*

81. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, WDS250G2B0A comprises TLC (triple level cell) flash technology. *User Manual* at 2. The SSD is configured to erase TLC blocks. *Id*. at 4; *White Paper* at 8.

82. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, WDS250G2B0A is configured to erase SLC blocks. *User Manual* at 4-5.

83. The Accused Products include a flash translation layer (FTL). For example, WDS250G2B0A contains a Flash Transition Layer (FTL). *SanDisk Presentation* at 17.

84. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, the FTL in WDS250G2B0A uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *White Paper* at 12. The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit. *White Paper* at 6, 8.

85. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next

available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, the flash memory in WDS250G2B0A is prone to read and write disturb errors. *White Paper* at 9. The FTL implements flash management techniques to address data integrity issues by remapping data. *Id*. at 4; *User Manual* at 4.

86. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, the FTL in WDS250G2B0A determines "hot" data and "cold" data. Hot data is stored in SLC memory and cold data is stored in MLC memory. *SanDisk Presentation* at 17, 19, and 20. The FTL maintains a hot count of each of the physical blocks. *White Paper* at 12.

87. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. For example, the FTL in WDS250G2B0A determines "hot" data and "cold" data and stores the "hot" data in the SLC memory. *SanDisk Presentation* at 20.

88. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

89. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

90. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '385 patent by Defendants.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 9,997,240

91. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

92. Defendants have directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 6 of the '240 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

93. The Accused Products meet all the limitations of at least claim 6 of the '240 patent. Specifically, claim 6 of the '240 patent recites:

> 6. A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
>
> wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only

receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

wherein the controller is further adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

94. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, WDS250G2B0A is a SSD for storing data. *Western Digital Store; see also White Paper at 1, 4.*

95. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, WDS250G2B0A comprises TLC (triple level cell) flash technology. *User Manual* at 2. The SSD is configured to erase TLC blocks. *Id*. at 4; *White Paper* at 8.

96. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, WDS250G2B0A is configured to erase SLC blocks. *User Manual* at 4-5.

97. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the

list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, WDS250G2B0A contains a controller with a NAND interface. *Controller*. The controller uses nCache technology. *nCache 2.0*; *nCache 3.0*. The controller uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *White Paper* at 12. The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit. *Id*. at 6, 8.

98. In the Accused Products, the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks. For example, the controller in WDS250G2B0A determines "hot" data and "cold" data and stores the "hot" data in the SLC memory. *SanDisk Presentation* at 20.

99. In the Accused Products, the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, the flash memory in WDS250G2B0A is prone to read and write disturb errors. *White Paper* at 9. The controller implements flash management techniques to address data integrity issues by remapping data. *Id*. at 4; *User Manual* at 4.

100. In the Accused Products, the controller is adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a

predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller. For example, the controller in WDS250G2B0A determines "hot" data and "cold" data. Hot data is stored in SLC memory and cold data is stored in MLC memory. *SanDisk Presentation* at 17 and 19-20. The controller maintains a hot count of each of the physical blocks. *White Paper* at 12.

101. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

102. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

103. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '240 patent by Defendants.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 10,950,300

104. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

105. Defendants have directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '300 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available, and Vervain reserves the right to identify additional infringing activities,

products, and services, including, for example, on the basis of information obtained during discovery.

106. The Accused Products meet all the limitations of at least claim 1 of the '300 patent. Specifically, claim 1 of the '300 patent recites:

> A system for storing data comprising:
>
> memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;
>
> at least one controller to operate memory elements and associated memory space;
>
> at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;
>
> at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;
>
> at least one random access volatile memory;
>
> an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;
>
> the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;
>
> the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory;
>
> wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and
>
> wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical

addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

107. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, WDS250G2B0A is a SSD for storing data. *Western Digital Store; see also White Paper at 1, 4.*

108. The Accused Products include memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space. For example, WDS250G2B0A contains volatile memory space. *nCache 2.0*; *nCache 3.0* at 11. The SSD also contains non-volatile memory space with both TLC and SLC memory space. *User Manual* at 2 and 4-5.

109. The Accused Products include at least one controller to operate memory elements and associated memory space. For example, WDS250G2B0A contains a controller with a NAND interface. *Controller*. The controller uses nCache technology. *nCache 2.0*; *nCache 3.0* at 11.

110. The Accused Products include at least one MLC nonvolatile memory element that can be mapped into the MLC memory space. For example, the controller in WDS250G2B0A uses an LBA mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *White Paper* at 11-12. The flash memory contains TLC memory space. *User Manual* at 2 and 4; *nCache 2.0*; *nCache 3.0* at 11.

111. The Accused Products include at least one SLC nonvolatile memory element that can be mapped into the SLC memory space. For example, the controller in WDS250G2B0A uses an LBA mapping table to keep track of the relationship between the logical blocks and the

physical addresses of the flash memory. *White Paper* at 11-12. The flash memory contains SLC memory space. *User Manual* at 5; *nCache 2.0*; *nCache 3.0* at 11.

112. The Accused Products include at least one random access volatile memory. For example, WDS250G2B0A contains random access memory (RAM). *nCache 2.0*; *nCache 3.0* at 11.

113. The Accused Products include an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory. For example, the controller in WDS250G2B0A contains a flash translation layer and uses an LBA mapping table to keep track of the relationship between logical block addresses of the operating system and physical addresses of the flash memory. *SanDisk Presentation* at 17; *White Paper* at 11-12.

114. The Accused Products include a controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory. For example, the controller in WDS250G2B0A controls access to the TLC and SLC memory and the RAM. *nCache* 2.0; *nCache 3.0* at 11. On information and belief, the controller stores data in the flash memory and retains data in the RAM. *White Paper* at 11-12.

115. In the Accused Products, the controller performs a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory. On information and belief, the controller in WDS250G2B0A performs a data integrity test by

comparing data stored in the flash memory with data retained in the RAM. *White Paper* at 11-12.

116. In the Accused Products, the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. For example, the controller in WDS250G2B0A provides wear leveling by remapping blocks of flash memory. *White Paper* at 11-12; *User Manual* at 4-5.

117. In the Accused Products, a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance. For example, the controller in WDS250G2B0A implements flash management techniques to address data integrity issues by remapping data. *White Paper* at 4, 11-12; *User Manual* at 4-5.

118. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

119. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

120. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '300 patent by Defendants.

REQUEST FOR A JURY TRIAL

121. Vervain requests a jury trial of all issues in this action so triable.

PRAYER FOR RELIEF

WHEREFORE, Vervain respectfully requests:

A. That Judgment be entered that Defendants have infringed one or more claims of the Asserted Patents, literally and under the doctrine of equivalents;

B. That, in accordance with 35 U.S.C. § 283, Defendants and all its affiliates, employees, agents, officers, directors, attorneys, successors, and assigns and all those acting on behalf of or in active concert or participation with any of them, be preliminarily and permanently enjoined from (1) infringing the Asserted Patents and (2) making, using, selling, and offering for sale, or importing into the United States, the Accused Products;

C. An award of damages sufficient to compensate Vervain for Defendants' infringement under 35 U.S.C. § 284;

D. That the case be found exceptional under 35 U.S.C. § 285 and that Vervain be awarded its reasonable attorneys' fees;

E. Costs and expenses in this action;

F. An award of prejudgment and post-judgment interest; and

G. Such other and further relief as the Court may deem just and proper.

Dated: May 10, 2021.

Respectfully submitted,

/s/ Alan L. Whitehurst

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